

REMARKS

Claims 1-10 and 19-30 are pending in this application, of which claims 1, 19-21, 25 and 30 have been amended. No new claims have been added.

Claims 1, 2, 7-10, 19-21 and 26-30 stand rejected under 35 USC §103(a) as unpatentable over **Tottori** or **Buynoski** (both previously applied) singly or in combination.

Applicant respectfully traverse this rejection.

Tottori discloses a semiconductor device with a multi-level interconnection structure having a first conductive layer 32 disposed below a fuse 31, and formed in the same layer as the first metal wire as a component of multi-level interconnects, and a second conductive layer 33 disposed below the fuse 31 and formed in the same layer as the second metal wire as a component of the multi-level interconnects. These conductive layers are used for absorbing a laser beam but are not used for normal wiring.

Neither **Tottori** nor **Buynoski** disclose a conductive layer not connected to a stack VIA but which is used for normal wiring, as claimed in the present invention. Thus, neither reference teaches, mentions or suggests improving wiring efficiency because neither provides an intermediate metal layer wiring area adjoining an intermediate metal layer for two layers connected with a stack VIA, as in the present invention.

Accordingly, claims 1, 19-21 and 30 have been amended to recite this distinction and the 35 USC §103(a) rejection should be withdrawn.

U.S. Patent Application Serial No. 09/855,590
Response to Office Action dated February 12, 2004

In view of the aforementioned amendments and accompanying remarks, claims 1-10 are now in condition for further examination.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: RCE
Petition for Extension of Time

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